Novel loop architectures for enhancing linearity and resolution of analog-to-digital converters

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Abstract — This paper proposes three mixed (analog and digital) loop architectures which involve an analog-to-digital converter and enhance its linearity and its resolution. Their benefits are discussed with mathematical models and high-level simulations (the ADC inserted in the loops is then a passive sigma-delta structure). One of the loop topologies is particularly highlighted: it is ideally able to enhance resolution by 5 bits without damaging bandwidth. The only added analog element is an active differential low-pass filter. The other operators are fully digital: a predictor and some models of the analog parts. The effect of some defaults, such as mismatch and common mode, is illustrated by high-level simulations. The needed accuracy for the digital parameters is evaluated to 16 bits. The test of a prototype realized in a 0.35µm CMOS technology validates the principle and demonstrates that the critical element of the structure is the active differential filter.

Keywords: analog-to-digital conversion, sigma-delta, linearity, resolution, consumption

1. Introduction

Among the various types of analog-to-digital converters (ADC), sigma-delta (ΣΔ) structures are able to provide the highest resolution (more than 24 bits) compared with flash, pipeline or SAR converters. This is paid with a lower bandwidth (below 100 kHz). These performances dedicate sigma-delta structures to an extensive use for several applications such as digitizing audio signals. Yet, the active low-pass filters involved in traditional sigma-delta structures damage consumption. That is why some research has been performed about passive ΣΔ structures [1-5]. In such converters, the only analog active element is a comparator. Consequently, the consumption of passive sigma-delta converters is potentially lower than any other kind of analog-to-digital converters. The negative points of these structures are their linearity, resolution and bandwidth which are lower than those of active sigma-delta structures. Thus, passive sigma-delta converters are placed between pipeline and SAR converters as far as resolution is concerned.

In this paper, we propose and discuss three architectures which are able of improving linearity and resolution of an analog-to-digital converter. They derive from control theory: the principle is to keep the ADC input signal closed to the mid-point of its full scale, which is the point where the non-linearity error is the lowest. Such topologies can theoretically be used for any converter exhibiting low linearity and resolution. In the article, they are tested with a passive sigma-delta converter.

Two of the proposed loop topologies are directly derived from basic concepts of control theory. They add few operators to the converter. They both enhance linearity and resolution but this increment is paid with a bandwidth reduction. The good point is that all the supplementary elements are digital, which preserves low consumption. The second topology complements the previous one with an active low-pass analog filter. Resolution and linearity are increased compared with the simplest topology, but consumption is also higher. This paper proposes a third architecture which is original and outstanding since it ideally provides an increment of 5 bits compared with a single converter, without damaging bandwidth. It is a little more complex than the two others, since it also involves some digital models of the analog parts.

On the base of these topologies, it is possible to build converters able to work in several different modes. For example, in the "low consumption mode", a passive sigma-delta converter is used alone. In the "high resolution mode", it is inserted in a loop topology in order to increase resolution. An application for two-mode converters (either a low consumption with low resolution, either mid resolution with little more consumption) can be found in mobile phones for example. The autonomy of the battery is one of the critical points in mobile communication systems. A steady monitoring of the supply level is required, which makes very low-consumption A/D converters necessary. For that, the resolution constraints can be relaxed for most of the measurements ("low consumption mode"). However, conversions with higher resolution have to be performed from time to time for more accurate measurements ("high resolution mode"). This mode could also be used for other selective applications, such as audio conversion. Thus, a versatile ADC, capable of operating in two different modes (instead of two ADC), could help reduce the overall consumption and area.

The paper is organized as follows. In Section 2, a high-level description of the three loop topologies is given. Their functioning is analyzed with a simple mathematical model. High-level simulations results are developed in Section 3. They highlight the achievable enhancements as well as the limitations of each topology and prove that the last one is the most original and promising. Further simulation results about this topology evaluate its sensitivity towards mismatch or towards the defaults of the analog part. Before concluding, we show in Section 4 some experimental measurements obtained with an integrated CMOS prototype.

2. Loop architectures: high-level description and simple mathematical model

In this section, three loop architectures are described at high level. They include an ADC and build, with this ADC and some additional elements, a "new ADC". Their principle is analyzed on the base of a simple mathematical model that will be consolidated in Section 3 with high-level simulation results. The two first topologies are directly derived from basic concepts of control theory. The pros as well as the cons of these structures are analyzed. A new topology is then proposed in order to enhance the performances.

2.1. Fully passive loop topology

The principle of loop topologies is to put the A/D converter in a servo-control loop in order to keep its input signal closed to the mid-point of the full scale, the point for which the non-linearity error is the lowest. According to basic concepts of control theory [6], this can be made by inserting an integrator in the loop, resulting in the topology shown in Fig. 1. The ADC is followed by a digital integrator (*Int(z)*). A DAC in the feedback path is mandatory. It can be an active digital sigma-delta converter. Such DAC are composed with two stages: a digital sigma-delta modulator and an analogue low-pass filter. The latter might not be necessary since the ADC generally behaves as a low-pass filter. In this case, this loop only adds digital elements to the ADC, no further analog active elements (that is why we call it "fully passive"), which simplifies the circuit and preserves a low consumption. Finally, the whole loop builds a "new ADC" (as mentioned in Fig. 1).

A rigorous model of the loop is not quite easy to calculate since this system is both non-linear and multi-cadenced. Indeed, the sigma-delta modulator in the feedback path uses oversampling rate compared with the other operators. Besides, one could use different sampling frequencies for the ADC and for the digital integrator (this will be investigated in section 2.2).

Yet, in order to roughly understand how this topology works, a simple model can be used on the base of two hypotheses. First, classical linear models are used for the non-linear systems, ADC and DAC (Fig. 2):

- $T_1(z)$ is the ADC signal transfer function; it is roughly 1 in the band;
- $B_1(z)$ is the quantization noise induced by the ADC (B_1 can be white or shaped noise according the ADC type);
- $T_2(z)$ is the DAC signal transfer function; it is roughly 1 in the band;
- $B_2(z)$ is the resulting quantization noise induced by the DAC;
- if there is no analog filter in the feedback path, $T_2(z)$ is the signal transfer function of the digital sigma-delta modulator; $B_2(z)$ is the quantization noise induced by the digital sigma-delta modulator.

Secondly, the converter input signal is supposed to be a sampled and held signal at the lower cadence of the system. The expressions of $C(z)$ and $A(z)$ as a function of $\varepsilon(z)$ and $O(z)$ respectively are:

$$C(z) = T_1(z)\varepsilon(z) + B_1(z) \quad (1)$$

$$A(z) = T_2(z)O(z) + B_2(z) \quad (2)$$

$O(z)$ can easily be written as a function of $I(z)$, $B_1(z)$ and $B_2(z)$:

$$O(z) = \frac{Int(z)}{\left(1 + Int(z)T_1(z)T_2(z)\right)}\left(T_1(z)I(z) - T_1(z)B_2(z) + B_1(z)\right) \quad (3)$$

If $Int(z) = \frac{kz^{-1}}{1 - z^{-1}}$, it leads to:

$$O(z) = \frac{kz^{-1}}{1 - \left(1 - kT_1(z)T_2(z)\right)z^{-1}}\left(T_1(z)I(z) - T_1(z)B_2(z) + B_1(z)\right) \quad (4)$$

For low frequencies, the signal transfer function is equal to $\frac{1}{T_{2\_DC}}$ (T_{2_DC} is the DC gain of $T_2(z)$). This is a very positive point since the DC signal gain is no more related to the ADC gain T_{1_DC} (non-linear for a mediocre ADC): it is directly related to the digital sigma-delta DC gain T_{2_DC} (more linear).

On the other hand, the noise transfer functions are equal (for $B_2(z)$) or similar (for $B_1(z)$) to the signal transfer function. This means that a reduction of $B_1(z)$ and $B_2(z)$ would be paid with a bandwidth reduction.

Further information can be easily extracted from Eq. 4 provided few approximations are used. Thus, T_{1_DC} and T_{2_DC} are approximately equal to 1. Consequently, within the passband of T_1 and T_2, Eq. 4 results approximately in:

$$O(z) \approx \frac{kz^{-1}}{(1 - (1 - k)z^{-1})}\left(I(z) - B_2(z) + B_1(z)\right) \quad (5)$$

which means that:

- k has to be inferior to 1 for stability reason;
- the input signal as well as the quantization noises are filtered by a low-pass filter the cut-off frequency of which is about $F_c = \frac{F_s}{2\pi}\frac{k}{(1-k)}$ (this conclusion is valid only if F_c is within the bandpass of T_1 and T_2).
- For frequencies superior to F_c (and within the passband of T_1 and T_2), the noise and signal transfer functions tend towards $\frac{k}{2-k}$.

It can be deduced from these rough considerations that *k* should not exceed a certain value for stability reason and a compromise should be found, since the lower *k*, the lower the noise but also the lower the bandwidth.

2.2. Active topology

Considering $B_1(z)$ as a perturbation, control theory shows that its impact on the output $O(z)$ can be reduced with the adjunction of an amplifier preceding the ADC. It results in the topology in Fig. 3. Actually, an active filter has been added instead of an amplifier because this operator is also used as an analog low-pass filter to reduce $B_2(z)$ (quantization noise due the DAC in the feedback path). Consequently, in Fig. 3, only the DAC first stage (a digital sigma-delta modulator) is kept, which simplifies design and reduce circuit area and consumption. A digital attenuation of $1/G''$ is also added in the loop. The aim is to keep the same DC gain in the direct path as in the previous structure, which means that G'' should be equal to G.

A linear mathematical model for this "new ADC" can be extracted from the same hypotheses as for the previous topology (see linear models in Fig. 3). The active filter noise ($B_3(z)$) is also introduced, which gives:

$$O(z) = \frac{Int(z)}{\left(G'' + Int(z)F(z)T_1(z)T_2(z)\right)}\left(F(z)T_1(z)I(z) + B_1(z) - F(z)T_1(z)B_2(z) + T_1(z)B_3(z)\right) \quad (6)$$

Like in the previous topology, the DC signal gain is $\frac{1}{T_{2\_DC}}$, which means that the linearity of this "new ADC" is improved compared with the ADC within the loop. In the passband of T_1 and T_2, and considering $G = G''$, Eq. 6 results in:

$$O(z) \approx \frac{kz^{-1}}{\left(1-(1-k)z^{-1}\right)}\left(I(z) + \frac{B_1(z)}{G} - B_2(z) + \frac{B_3(z)}{G}\right) \quad (7)$$

Equations (5) and (7) show the increment of this topology in comparison with the previous one: it divides by G the quantization noise of the passive modulator ($B_1(z)$). Note that $B_3(z)$ is also divided by G.

2.3. Enhanced active topology

2.3.1. Description and simple mathematical model

The previous topology exhibits a potential high resolution but the impact of $B_2(z)$ is not reduced. Besides, a compromise should be found between bandwidth and resolution. To correct these defaults, we propose the topology shown in Fig. 4. The integrator ($Int(z)$) has been replaced here by a predictor ($P(z)$) in order to preserve bandwidth by compensating in the feedback path the delay introduced by the direct path. Digital models of the analog parts ($F'(z)$ and $T_1'(z)$) aim at reducing the noise introduced by the digital modulator ($B_2(z)$).

A simple mathematical model based on the same hypotheses as for the previous topologies (see linear models in Fig. 4). highlights how this architecture operates. Output signal $O(z)$ is expressed as a function of input signal $I(z)$:

$$O(z) = \frac{1}{\left(G'' + A(z)P(z)T_2(z)\right)}\left(F(z)T_1(z)I(z) + B_1(z) + A(z)B_2(z) + T_1(z)B_3(z)\right) \quad (8)$$

where $A(z) = F(z)T_1(z) - F'(z)T_1'(z)$.

The DC signal gain is approximately equal to $\frac{GT_{1\_DC}}{G'' + GT_{2\_DC}T_{1\_DC} - G'T_{1\_DC}'T_{2\_DC}}$. Thus, if $G'' = G'T_{1\_DC}'T_{2\_DC}$, the DC signal gain is equal to $\frac{1}{T_{2\_DC}}$, which means that the linearity is improved compared with the ADC within the loop.

Besides, if $A(z)$ is null (which means that the digital model perfectly matches the analog parts and in particular: $GT_{1\_DC} = G'T_{1\_DC}'$), Eq. 8 gives:

$$O(z) = \frac{1}{G''}\left(F(z)T_1(z)I(z) + B_1(z) + T_1(z)B_3(z)\right) \quad (9)$$

Thus, the quantization noise of the feedback modulator and as well as the amplifier noise are divided by G'' (just like in the previous topology). Besides, the increment of this topology is that the effect of $B_2(z)$ is cancelled.

It can be seen in Eq. 9 that bandwidth is limited by the cut-off frequencies of $T_1(z)$ and $F(z)$. This means that it is inferior or equal to the bandwidth of the ADC inside the loop. To make it equal the cut-off frequency of $F(z)$ should be taken high enough, which exhibits theoretically no drawbacks.

2.3.2. Influence of mismatch

The topology operates ideally provided $A(z)=0$ and $G^{"}=G^{'}T_{1\_DC}^{'}T_{2\_DC}$. Let us now suppose that $A(z)$ is not perfectly null. The static gain towards B_2 is then $\frac{A_{DC}}{G^{"}+A_{DC}} \approx \frac{A_{DC}}{G^{"}}\left(1-\frac{A_{DC}}{G^{"}}\right)$. This topology is still quite interesting since B_2 is still much attenuated. It does not have any impact on the static signal gain if $G^{"}=G^{'}T_{1\_DC}^{'}T_{2\_DC}$. On the other hand, if ε is the relative mismatch between $G^{"}$ and $G^{'}T_{1\_DC}^{'}T_{2\_DC}$ then it results in a static signal gain equal to $\frac{1}{T_{2\_DC}}\left(1-\frac{\varepsilon}{T_{1\_DC}}\right)$. Therefore, it can alter linearity, but non-linearity error is likely to be lower than if the ADC within the loop is used alone. Anyway, the matching of $G^{"}$ and $G^{'}T_{1\_DC}^{'}T_{2\_DC}$ only concerns digital elements, which means that it is easy to achieve provided these elements are encoded with enough accuracy (this accuracy is determined by simulations in section 3.4.4: it is 16 bits).

2.3.3. Influence of the common mode of the active filter

Common-mode of the active filter is modeled as two different transfer functions, named $F_1(z)$ and $F_2(z)$, respectively towards or the positive and negative inputs. It results in:

$$O(z)=\frac{1}{\left(G^{"}+A(z)P(z)T_2(z)\right)}\left(F_1(z)T_1(z)I(z)+B_1(z)+A(z)B_2(z)+T_1(z)B_3(z)\right) \qquad (10)$$

where $A(z)=F_2(z)T_1(z)-F^{'}(z)T_1^{'}(z)$.

If $G^{"}=G^{'}T_{1\_DC}^{'}T_{2\_DC}$, the DC signal gain is $\frac{G_1}{G_2}\frac{1}{T_{2\_DC}}=\frac{G_{dm}+\frac{G_{cm}}{2}}{G_{dm}-\frac{G_{cm}}{2}}\frac{1}{T_{2\_DC}} \approx G_{dm}\left(1+\frac{G_{cm}}{G_{dm}}\right)\frac{1}{T_{2\_DC}}$

where G_{dm} and G_{cm} are respectively the differential mode gain and the common mode gain. Thus, the common mode of the active filter directly impacts the static signal gain and might damage linearity. This effect can be limited by designing a differential active filter with a high common-mode rejection ratio. Another possibility consists in choosing: $G^{"}=G_1T_{1\_DC}$ and $G_2T_{1\_DC}=G^{'}T_{1\_DC}^{'}$ (in fact: $F_2(z)T(z)-F^{'}(z)T^{'}(z)=0$). The DC signal gain is then equal to 1. However, this matching supposes that the analog part is known with enough accuracy. In-situ identification techniques might be necessary.

2.3.4. Influence of the predictor

The previous model does not show the impact of the predictor on the loop. The latter should give the best possible prediction of the input signal from the output signal, in order to use the passive sigma-delta modulator in its linear zone. Let us express $I_{ADC}(z)$, input signal of the ADC if $A(z)$ is null:

$$I_{ADC}(z)=F(z)\left[\left(1-\frac{P(z)T_2(z)F(z)T_1(z)}{G^{"}}\right)I(z)-\frac{P(z)T_2(z)}{G^{"}}B_1(z)-B_2(z)\right] + \left(1-\frac{P(z)T_2(z)F(z)T_1(z)}{G^{"}}\right)B_3(z) \qquad (11)$$

$I_{ADC}(z)$ should be as low as possible to enhance linearity, which means, considering the input signal contribution, that $P(z)$ should be ideally calculated in order to get in the signal band:

$$J(z)=1-\frac{P(z)T_2(z)F(z)T_1(z)}{G^{"}}=0 \qquad (12)$$

3. High-level simulation results

This section presents some high-level simulation results which consolidate the previous theoretical considerations. The ADC put inside the loop architectures is a passive sigma-delta converter. Its architecture as well as its performances will not be discussed in detail, since the topic of the paper is not passive sigma-delta converters. Actually, the loop architectures build a new ADC and the performances of the passive sigma-delta ADC only serve as reference to analyze and to comment the benefits they provide. Some results about the two first topologies will be briefly presented. We will then focus on the enhanced active topology, which is the most original. Its increments compared with the previous architectures will be highlighted and the critical points identified. Finally, a conclusion will summarize and discuss the whole results.

For each ADC configuration, we are exposing in this section some results of:

- transient simulations with a varying static input:
  - this leads to INL (integral nonlinearity) error, which is the deviation of the actual DC transfer function from a straight line; we name "DC error" the deviation if the reference straight line is the ideal one and "INL error" the deviation if the reference straight line is the one that fits the best the actual curve (this technique is very commonly used); note that INL error is indeed the achieved DC error if a linear (gain and offset) post-correction is performed after the ADC.
  - the output residual noise is also measured (the output signal of a sigma-delta converter is generally not static even for an static input); indeed, this noise is not harmonic distortion: it is related to SNHD (Signal to Non-Harmonic Ratio, named SNR by many manufacturers), which is usually measured with a sinus input;
  - ENOB (Effective Number of Bits) can be evaluated from the superposition of DC error and noise error; the superposition of INL error and noise error gives the achieved ENOB if a linear post-correction is performed;
- step responses: though such stimulations are not standardized, they provide a good graphical illustration of some effects in the loop topologies;
- sinus responses: this leads to bandwidth and SINAD (SIgnal-to-Noise And Distorsion ratio), expressed as an Effective Number Of Bits (ENOB). ENOB calculated with sinus responses, as described in standard 1241, should be in good agreement with ENOB derived from simulations with a static input.

3.1. Passive sigma-delta converter

3.1.1. Description

In this paper, the mediocre ADC chosen as a reference is a passive sigma-delta structure. The design of a passive low-pass discrete-time second-order sigma-delta converter has already been presented [7]. Since the topic of the paper is not passive modulation but how a mediocre ADC can be improved by external elements, we are focusing here on the resulting architecture (Fig. 5). Like its active counterparts, it is composed with two elements: the sigma-delta modulator and a digital filter. The modulator is a classical one-loop sigma-delta structure. It is composed with a discrete-time low-pass filter (passive here) and a triggered comparator in the direct path, complemented with a 1-bit DAC in the feedback path. The filter coefficients (a_i and b_j in the transfer function $M(z)$) result from a compromise between resolution and stability on one hand and the signal level at the comparator input on the other hand. Actually, if the latter is too low, a comparator capable of processing it can not be physically realised. Previous studies [7] led to: $a_0 = 0$; $a_1 = 0.0064$; $a_2 = -0.00452$; $b_0 = 1$; $b_1 = -1.885$; $b_2 = 0.887$. Note that a dither signal (a white noise of mean value 0 and variance 0.001) is added at the comparator input: this is a classical technique used in sigma-delta structures to suppress the dead zone around the mid-point (a zone in which some inputs cannot be precisely quantized so that the ADC outputs a zero) [8]. As far as the digital filter is concerned, we chose a simple one. Its global decimation ratio is 256: the output samples are delivered at a rate of $F_s/256$. Its cut-off frequency is $F_s/610$, where F_s is the sampling frequency of the modulator. Lastly, note that the full scale is normalized between -1 and 1, which means that the two values delivered by the 1-bit DAC (modulator feedback signal) are -1 and 1.

3.1.2. Static performances

ADC linearity and resolution can be evaluated from high-level transient simulations with a static input signal. Fig. 6 shows the deviation between the actual DC transfer function of the passive sigma-delta converter and the ideal transfer function. It is indeed the difference between the input signal and the mean value of the modulator feedback signal:

- the input signal is the analog value that should ideally corresponds to the digital ADC output (more precisely: to its DC value, since there is an additional noise at the output);
- the mean value of the modulator feedback signal is the analog value which actually corresponds to the mean value of the ADC digital output.

This difference is named here DC error. It should be null in the ideal case, and linear if the modulator is linear (in that case, there is only a gain and/or offset error). Note that the modulator non-linearity appears clearly. DC error, INL error and residual noise at the digital filter output are presented in Fig. 7, both expressed with an equivalent number of bits. The equivalent number of bits is the equivalent resolution if the considered error (DC, INL or output noise) is supposed to be the only error and equal to 1 LSB.

The output residual noise is superior to 11.2 bits for an input signal between -0.8 and 0.8 and 9.4 bits between -1 and 1. The DC error goes down to 8.4 bits between -0.8 and 0.8, and down to 7.2 bits between -1 and 1. After a linear post-correction (INL error), it is 11.2 bits for an input signal between -0.8 and 0.8 and 8.1 bits between -1 and 1. This results in a global ENOB of 8.2 bits (10.2 bits with a linear correction) between -0.8 and 0.8 and 7.1 bits (7.9 bits with linear correction) within the full range.

Besides, some simulations introducing a relative error of 20% in coefficients a_i and b_j show it does not affect the results presented above. A practical consequence is that in-situ identification techniques are not required for implementing the linear post-correction. This can be done on the base of simulation results.

3.1.3. Dynamic performances

Step response

The step response of the passive sigma-delta converter (modulator and digital filter) and of the digital filter alone are plotted in Fig. 8 with F_s = 10 MHz and an input step of 0.5. Both responses are closed, which indicates that response time and bandwidth are limited here by the decimation filter and not by the modulator.

Sinus response

The power spectral density of the modulator output is plotted in Fig. 9. The input signal is a sinus of amplitude 1, offset 0 and frequency 5 kHz. It illustrates that the passive modulator, just like classical active sigma-delta modulators, performs a noise shaping (noise is rejected to high frequencies).

ENOB (standard 1241) was evaluated with a pure sine wave input of magnitude 0.5 for various frequencies. As expected from static performances, it is about 8 bits in the digital filter band (without linear post-correction). Bandwidth is thus imposed by the digital filter: it is $F_s/610 \approx$ 16kHz.

3.2. Fully passive loop topology

The passive sigma-delta converter shown in Fig. 5 is inserted in a fully passive topology (Fig. 1). The digital modulator in the feedback path is a classical second-order one [8]. Its sampling frequency is taken equal to F_s. The analogue low-pass filter that could follow the digital modulator is suppressed for simplicity and consumption reasons and considering that the passive converter also behaves as a low-pass filter.

We are showing below some results that evaluate the potential performances of this architecture and illustrate the influence of two parameters related to the digital integrator: the k coefficient and the decimation ratio towards F_s, named r. k is written as a power of 1/2 ($k=1/2^n$, where n is an integer), which is preferable for realization simplicity. If r = 256, simulations show that the loop is stable only if k is inferior or equal to 1/8. It can also be observed by simulation that the maximal allowed value for k is an increasing function of r; such a result could be demonstrated with a more rigorous calculus than the one developed in the previous paragraph. Yet, it is not the purpose in this paper.

3.2.1. Step response

Fig. 10 and 11 present the step response of the loop with F_s = 10 MHz and an input step of 0.5. In Fig. 10, r is fixed (r = 256) and the influence of k is observed. Fig. 10(a) focuses on the transient period and shows that the loop behaves as a second-order system with a damping factor proportional to 1/k. The optimal value of k to minimize the response time is 1/16. Fig. 10(b) illustrates the steady state. It shows that the higher k, the higher the quantization noise. This observation agrees the mathematical model (Section 2.1). Fig. 11 illustrates the loop step response for a fixed value of k (k = 1/16) and for different values of the decimation ratio r. Fig. 11(a) focuses on the transient period. As it could be expected, the higher the decimation rate, the higher the response time. Fig. 11(b) exhibits the steady state. It shows that r should be equal to 512 or 1024 to minimize the quantization residual noise. Thus, a compromise must be made between resolution and bandwidth to choose the parameters k and r. Note that k and r impact the output residual noise but not linearity (the DC value is kept the same). The minimum response time is obtained for k = 1/16 and r = 256. It is about 5 times higher than the one of the passive sigma-delta converter (Fig. 8), which means that this topology damages bandwidth.

3.2.2. Static performances

Fig. 12 represents the DC error and the output residual noise of the loop for k = 1/16 and r = 256 or 512. Like in the previous case, DC error is calculated from the difference between the input signal and the mean value of the output normalized between -1 and 1. It represents the deviation between the ideal and actual transfer functions. Note that if a linear post-correction is applied to this architecture, it does not change DC error, which means that there are no significant gain and offset errors. As a result, DC error and INL errors are equal.

It can be seen that r influences the dynamic range. A rail-to-rail structure is obtained with r = 512; INL error and output residual noise correspond to a minimal equivalent number of bits of 11.1 bits and 13.7 bits respectively. The minimal equivalent numbers of bits are approximately the same for r = 256 within the range [-0.8; 0.8]. It results in an ENOB of 11 bits. Compared with a passive sigma-delta converter using a linear post-correction, the increment is 3.1 bits within the full range and 0.8 bit within [-0.8; 0.8].

3.2.3. Sinus response

ENOB was evaluated with a pure sine wave input of magnitude 0.5 (k and r are taken equal to 1/16 and 256 respectively). As expected from static performances, it is about 11 bits within the band (without linear post-correction). Bandwidth is 5 times lower than thus imposed by the digital filter: it is F_s/610/ ≈ 3kHz.

3.3. Active topology

An active filter is added to the previous architecture to build the topology shown in Fig. 3. We will give below some results that evaluate the potential performances of this architecture and illustrate the influence of two parameters related to the active analogue low-pass filter: G and α coefficients. G is written as a power of 2 ($G = 2^n$, where n is an integer), which is preferable for realization simplicity. k and r are taken equal to 1/16 and 256 respectively.

3.3.1. Step response

Fig. 13 illustrates the loop step response for a fixed value of α (α = 10) and for different values of G, with F_s = 10 MHz and an input step of 0.5. It clearly shows that the higher G, the higher the response time and the lower the non-linearity error. A good compromise is G = 4, the response time is then approximately the same as with the passive topology. Fig. 14 presents the loop step response for a fixed value of G (G = 4) and for different values of α. The impact of α on the response time is less significant than G (Fig. 14(a)). However, it can be seen that the higher α, the higher the response time. Besides, α plays an important role in the linearity. The influence of G and α on linearity were not predicted by the linear mathematical model.

3.3.2. Static performances

Fig. 15 shows the INL error (which is equal to the DC error) and the output residual noise of the loop for $G = 4$ and $\alpha = 10$. The structure is not rail-to-rail. INL error and output residual noise correspond to a minimal equivalent numbers of bits of 16.2 and 15.2 respectively (between -0.9 and 0.9). The global resolution is 15.2 bits.

3.3.3. Sinus responses

ENOB was evaluated with a pure sine wave input of magnitude 0.5 ($G = 4$ and $\alpha = 10$ are taken equal to 4 and 10 respectively). As expected from static performances, it is about 15 bits within the band (without linear post-correction). Bandwidth is 5 times lower than thus imposed by the digital filter: it is $F_s/610/ \approx 3$kHz.

3.4. Enhanced active topology

3.4.1. Architecture description

The previous topology is modified to obtain the one presented in Fig. 16. Some changes have been introduced compared with the topology shown in Fig. 4:

- the digital filter *H(z)* has been factorized for realization simplicity;
- it has been divided in 2 operators ($H_1(z)$ and $H_2(z)$); only the first one is induced in the loop in order to reduce the delay by the direct path.

The predictor *P(z)* should ideally make *J(z)* null in the signal band (Eq. 12). It can be calculated considering that it should compensate the delay, named *d*, introduced by the direct path and by the digital modulator. The value of *d*, extracted by simulation, is 5 samples in our case. Several predictors have been thought of and tested (linear, parabolic, etc.). We are selecting below only three of them:

- a simple holder: $P_1(z) = 1$;
- a predictor based on a linear interpolation with two samples at t_n and t_{n-d}: $P_2(z) = 2 - z^{-d}$;
- a parabolic interpolator: $P_3(z) = 21 - 35z^{-1} + 15z^{-2}$.

$J(z)$ magnitudes for $P_1(z)$, $P_2(z)$ and $P_3(z)$ are plotted in Fig. 17. It suggests that among these three predictors, the parabolic interpolator is the most adequate. Yet, high-level simulations of the loop have shown it is likely to provoke unstability. Indeed, parabolic predictors act like 2nd-order low-pass filters with a low damping coefficient. Their step response does not maintain the modulator input around zero, which might cause its saturation. That is the reason why the linear interpolator is a good compromise all the more so as it is simpler to realize.

All the following results are given for $P(z) = P_2(z)$.

3.4.2. Ideal case

The structure presented in Fig. 16 was simulated for $G = 4$, $\alpha = 40$ and with a perfect matching, that is to say, the digital models is ideally matched with the analog parts ($F'(z) = F(z)$ and $T_1'(z) = T_1(z)$) and G'' is taken equal to $G'T_{1\_DC}'T_{2\_DC}$. DC error is presented in Fig. 18. DC error, INL error and output residual noise are plotted in Fig. 19. The structure is rail-to-rail. DC and INL errors are roughly equivalent and correspond to a minimal equivalent number of bits of 15. Output noise corresponds to a minimal equivalent number of bits of 14. It results in an ENOB of 13.6 bits within the full range.

3.4.3. Influence of mismatch

Fig. 20 shows the influence of a mismatch between G'' and $G'T_{1\_DC}'T_{2\_DC}$ on DC error, INL error and output noise. $F'(z)$ and $T_1'(z)$ are kept matched with $F(z)$ and $T_1(z)$ respectively. A relative mismatch error of 1% is introduced between G'' and $G'T_{1\_DC}'T_{2\_DC}$. Output noise is not affected (minimal equivalent number of bits: 13.9 bits). But DC error falls down to 7.6 bits within the full range. It is restored with a linear post-correction (see INL error). These results are in good

agreement with the mathematical model (Section 2.3.2). ENOB (without a linear post-correction) is plotted in Fig. 21 as a function of the relative mismatch error. It decreases drastically when the mismatch exceeds 0.01%, which means it is a critical point of the structure. The mismatch should be kept below 0.001% to preserve 14 bits of resolution. This indicates that digital parameters should be coded with at least 16 bits.

The effect of a mismatch between the digital models and the analog parts is illustrated by Fig. 22. Here, a mismatch of 20% between the static gain of $F(z)T_1(z)$ and $F'(z)T_1'(z)$ is introduced. G'' and $G'T_{1\_DC}'T_{2\_DC}$ are kept matched. DC error (equal to INL error) and output residual noise correspond to a minimal equivalent number of bits of 15.2 and 13.2. As expected (see section 2.3.2), linearity is not affected. Output noise increases, but not so much. ENOB is 13.2 bits. This indicates that the dispersion of the analog elements does not have a significant impact on the structure.

3.4.4. Influence of common mode

The effect of the common mode of the analog active filter *F(z)* was analyzed, taking the common-mode gain constant (which means that the common mode is supposed linear).
Fig. 23 shows DC error, INL error and output residual noise in the following conditions: G'' and $G'T_{1\_DC}'T_{2\_DC}$ are kept matched; *G'* is matched to the differential gain of the active filter. If CMRR (common-mode rejection ratio) is 100dB (Fig. 23(a)), ENOB is kept above 13.4 bits within the full range (minimal DC error: 13.8 bits; minimal output noise: 13.6 bits). If CMRR is 40dB, output noise is not affected (minimal equivalent number of bits: 14.1 bits) but DC error is drastically damaged and ENOB falls down to 7.6 bits. With a linear post-correction, a DC error above 13.9 bits is restored (see INL error) and ENOB is drawn up to 13.2 bits. This is in good agreement with Section 2.3.3 which predicted that the common mode – if linear – should increase the converter gain error.

ENOB within the full range without a linear post-correction is represented as a function of CMRR in Fig. 24. CMRR is to be around 100dB to preserve the ideal ENOB (13.6 bits).

The mathematical model in Section 1 indicates that the common-mode effect can also be corrected by matching G'' to $G_1T_{1\_DC}$ and $F(z)$ to $F_2(z)$ (G_1 is the gain toward the positive input, $F_2(z)$ is the transfer function towards the negative input). This matching leads to the performances shown in Fig. 25. The CMRR is 40dB. Fig. 25(a) shows that if the matching is perfect, the performances of the ideal case are restored. In Fig. 25(b), a mismatch relative error of 20 % is introduced in $F(z)$. It demonstrates that this architecture is likely to be sensitive towards analog dispersion.

3.4.5. Dynamic performances

Step response

Fig. 26 presents the step response of the architecture, ideal or with some defaults (mismatch, common mode) and compares it with the step response of the passive sigma-delta converter alone. It can be seen that mismatch (of G'' or of the digital models) and common mode do not have any significant impact on the step response of the architecture, which remains closed to the step response of the passive sigma-delta converter. This is in good agreement with theoretical considerations in Section 2.3.1.

Sinus response

ENOB is evaluated with a pure sine wave input of magnitude 0.5 in the ideal case. As expected from static performances, it is about 13 bits within the band (without linear post-correction). Bandwidth is about 16kHz.

3.5. Conclusion and discussion

Table 1 summarizes ENOB and bandwidth of the previous architectures: passive sigma-delta ADC alone and when inserted in one of the loop architectures. The performances are not important for themselves, but the differences between the loop topologies and the single passive sigma-delta ADC. Note that:

- linear post-correction increases ENOB of the passive ADC alone but not of the loop topologies; this means that the loop topologies do not exhibit any gain or offset error, even though the ADC inside does;
- the performances of the loop architectures are given after choosing the parameters (k, r, G, α) in order to achieve a compromise between bandwidth and resolution; consequently, higher ENOB is achievable but it will be paid by a bandwidth reduction;
- ENOB is given here for a special input value (0.5); for every architecture, it is roughly the same within the range between -0.8 and 0.8; yet, only the enhanced active topology is rail-to-rail.

Compared with the passive sigma-delta converter followed by a linear post-correction, the fully passive topology is not so interesting, since it enhances resolution by 1 bit but divides bandwidth by 5. Besides, it involves more digital elements than a digital linear post-correction. Consequently, consumption is likely to be higher.

The active topology provides an interesting increment of ENOB (5 bits) but bandwidth is divided by 5. It is interesting to compare this topology with another one which would have roughly the same analogue consumption: a first-order active sigma-delta converter built with the active analog filter $F(z)$. Such a structure exhibits 7 bits of ENOB and 16 kHz of bandwidth. This illustrates that the active topology is an attractive candidate for high-resolution low-bandpass applications.

Yet, the full passive topology and the active topology are not so original. First, their structure is very similar to sigma-delta or delta modulators. Indeed, in both topologies, like in sigma-delta modulators, an ADC is involved in a loop with an integrator. The full passive topology is closed to a first-order sigma-delta modulator (one integration in the loop) whereas the active topology is similar to a second-order one (two integrations in the loop). One difference with classical sigma-delta structures is the feedback path: it is not a DAC but a digital sigma-delta modulator, which is a good point for design and consumption reasons. As far as performances are concerned, both topologies, like sigma-delta converters, increase resolution but decrease bandwidth. The conclusion of this parallel is that these topologies are not so innovative in their principles. Besides, their benefits compared with traditional sigma-delta converters have not yet been demonstrated.

Actually, the enhanced active topology is both innovative and promising. The structure is innovative. It derives from the two other topologies, therefore it is also closed to sigma-delta principle. Yet, the innovation is additional digital models of the analog parts and the use of a predictor instead of an integrator. The benefits are also innovative: this architecture enhances significantly ENOB without decreasing bandwidth.

4. Circuit design and measurement results

4.1. Circuit design

A prototype circuit was realized in order to validate some of the principles presented previously and to point out some limitations. The objective was a converter able to operate in two different modes. In the “low consumption mode”, the modulator is simply followed by a low-pass digital filter which also decimates the signal, to build the converter. In the “high resolution mode”, the passive sigma-delta converter is inserted in a loop topology (we chose the enhanced active topology). The designed modulator and loop topology are represented in Fig. 5 and Fig. 16).

The digital part was defined as a HDL code and implemented in an Altera board. The analog parts were integrated in the AMS 0.35µm technology. The chip is composed with: the comparator; the passive switched-capacitor low-pass filter; the active switched-capacitor filter; the $V_{DD}/2$ reference generators (virtual ground) where V_{DD} is the supply voltage; a digital part using standard cells (essentially switches command). The comparator, the passive filter and the reference generators were previously presented [9]. The comparator was designed to minimize the consumption. The circuit operates a comparison on each rising clock edge and exhibits no

consumption when the clock is on low level. Consequently, a self-timed digital system is used in order to pull the comparator clock down to "0" as soon as the comparison is done. The resulting comparator has just a dynamic consumption depending on the sampling frequency F_s.

Due to the foundry schedule, the topology could not be fully investigated at system level and its sensitivity towards the common mode rejection ratio of the active filter had not been identified before the transistor level design. Therefore, regarding our objectives (validation and investigation), the choice criterion for the active filter circuit was simplicity (Fig. 27). The structure is single-ended and there is only one capacitor at the input. The transfer function is:

$$\frac{V_o}{(V_{i_1} - V_{i_2})} = \frac{-\frac{C_2}{C_3} z^{-1}}{1 + \frac{C_1}{C_3}\left(1 - z^{-1}\right)} \quad (13)$$

V_{i1} is the input signal to convert and V_{i2} is the feedback signal (delivered by the digital sigma-delta modulator). We took $\alpha = \frac{C_1}{C_3} = 40$ and $G = \frac{C_2}{C_3} = 8$. The minus sign of the transfer function is corrected digitally in the Altera Board. As V_{i2} is a binary signal, this input is connected to the ground or to V_{DD} by adequate switches. The signal reference (represented by a virtual ground in Fig. 27) is $V_{DD}/2$. It is produced by a switched-capacitor voltage divider.

This amplifier can be bypassed when the "low-consumption mode" is used. In this case, the biasing sources of the operational amplifier are switched off, in order to reduce the global consumption. The chip layout is shown in Fig. 28. Its area is 2mm×2mm. All the components are duplicated for test purpose.

4.2. Some measurement results

The measurement results we are giving were obtained in the following conditions: the supply voltage V_{DD} is 3.3 V; the decimation ratio of the digital filter H_1 is 256; the digital models are matched with the analog parts (G' is matched with the differential gain of the active filter); G'' and $G'T'_{1\_DC}T_{2\_DC}$ are also matched.

Fig. 29 gives INL error as a function of the DC input value (normalized between 0 and 1) for the passive converter (Fig. 29(a)) and for the enhanced active loop topology (Fig. 29(a)). A linear post-correction (gain and offset) is implemented in the Altera board. INL error of the passive converter is below 1.5×10^{-3} in the range [0.1; 0.9], which corresponds to an equivalent resolution of 9.3 bits. For the loop topology, it is below 4×10^{-4} in the range [0.1; 0.7] which corresponds to an equivalent resolution of 11.3 bits. Non-linearity increases drastically above 0.7 and below 0.1. Non-linearity error predicted by high-level simulations is 11.2 bits for the passive converter and 15 bits with the ideal loop topology, that is to say an increment of almost 4 bits. Thus, the experimental linearity of the passive converter as well as the increment of the loop topology (which is the topic of this paper) are not as much as expected (respectively 1.9 bit and 1.8 bit less). Besides, the conversion is not rail-to-rail. Concerning the first point, further analysis showed that it might be caused by charge injection effects and by the sensitivity of the comparator towards noise (because its input signal is low). Concerning the other points, they are likely to be provoked by the common-mode gain of the active filter. Its CMRR is 32 dB. High-level simulations have shown that if the common mode was linear, its effects should have been compensated by the linear post-correction, resulting in a non-linearity error of approximately 13.9 bits. Actually, it is not linear, and a correlation is observed between the non-linearity of the common mode gain of the active filter and the non-linearity of the loop topology (Fig. 30 and Fig. 29(b)).

The residual noise within the normalized range [0.1; 0.9] was evaluated to 9.6 bits for the passive converter and 12.3 for the loop topology. 11.2 bits and 14 bits respectively were expected. Thus the experimental increment of the loop is the one expected.

The measured bandwidth of the loop topology is about 15 kHz when the modulator sampling frequency is 8 MHz, which corresponds to the bandwidth of digital filter H_1. This is in agreement with high-level simulations.

The measured consumption for F_s = 1 MHz is 1.4 µA for the passive modulator and 173 µA for the input active filter. The consumption of the digital part on the Altera board can not be measured.

5. Conclusion

This paper proposes and discusses three mixed loop architectures: they involve an analog-to-digital converter and some others operators, thus building a new ADC with enhanced linearity and resolution.

The two first architectures directly derived from basic concepts of control theory. They both include a digital integrator (after the ADC) in the direct path and a digital sigma-delta modulator in the feedback path. One of these loops also involves an analog active differential filter (before the ADC). High-level simulations show that bandwidth is approximately divided by 5 when ENOB (within a reduced range) is increased by approximately 3 bit (simplest topology) or 8 bits (active one). The consumption of theses architectures is theoretically low, especially the simplest one, in which the only active analog element is a comparator. This makes them good candidates for applications such as steady state measurements (for example, monitoring of the battery level in a mobile phone). Both architectures are similar to sigma-delta or delta modulators: like in those structures, an ADC and an integrator are involved in the loop; the only innovation is the digital modulator used in the feedback path. Like classical sigma-delta techniques, these architectures increase resolution but it is paid with a bandwidth reduction. The benefits compared with classical sigma-delta techniques are still to be demonstrated.

The third proposed architecture has been derived from the two previous ones. Its principle is both innovative and promising. The digital integrator is replaced by a predictor and some digital models of the analog parts are added. Theoretically, this architecture should work with any type of ADC within the loop. It was tested with a passive sigma-delta ADC. High-level simulations show that ENOB is enhanced by 5 bits within the full range and bandwidth is not damaged, which is promising compared with classical sigma-delta techniques. Besides, the architecture is rail-to-rail and not very sensitive towards analog dispersion. The only critical point is that this topology requires a high-CMRR (100dB) active differential filter. A prototype of this structure was realized and tested. Measurements validate the principle and highlight that the critical element is the active analog filter and more precisely common-mode linearity.

Acknowledgements

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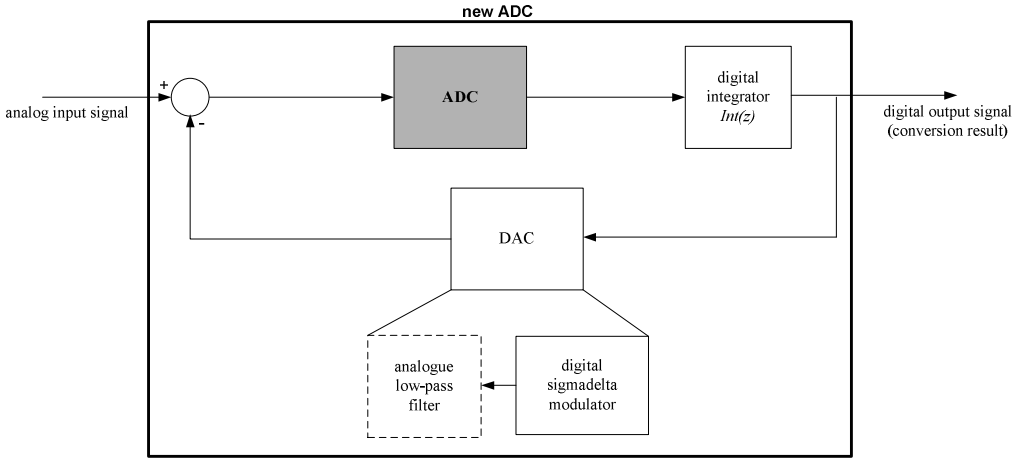


Fig. 1 Fully passive topology

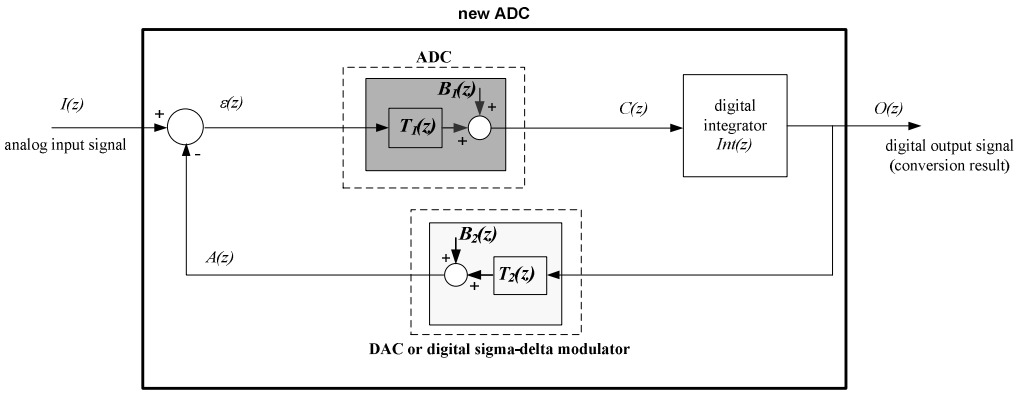


Fig. 2 Linear model of the fully passive topology

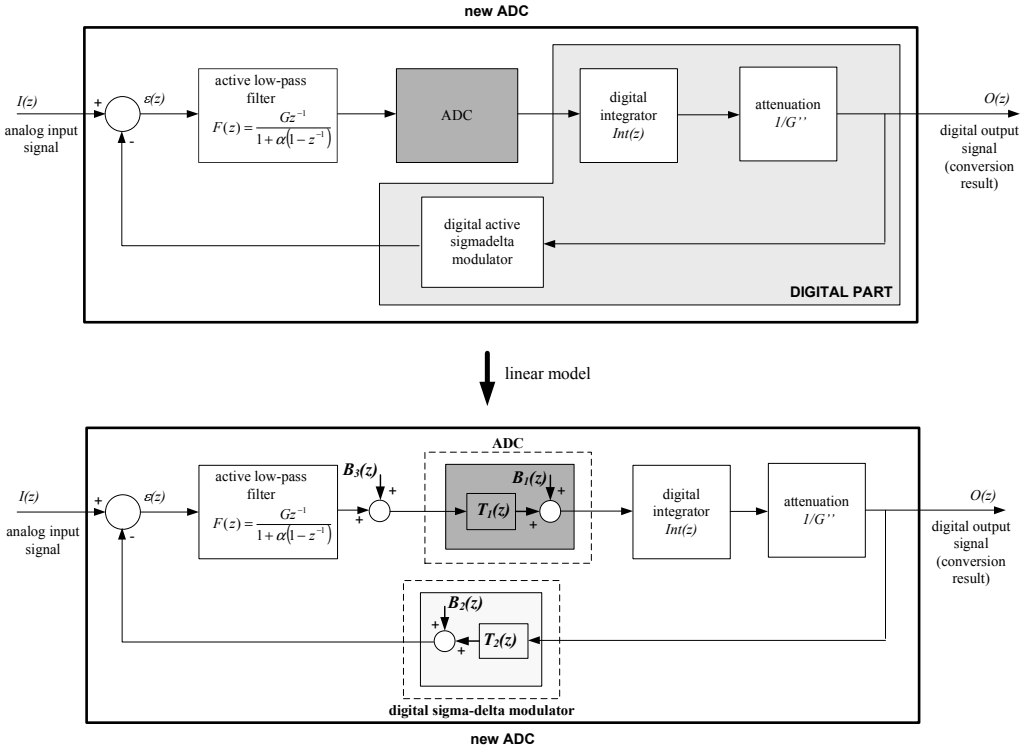


Fig. 3 Active topology

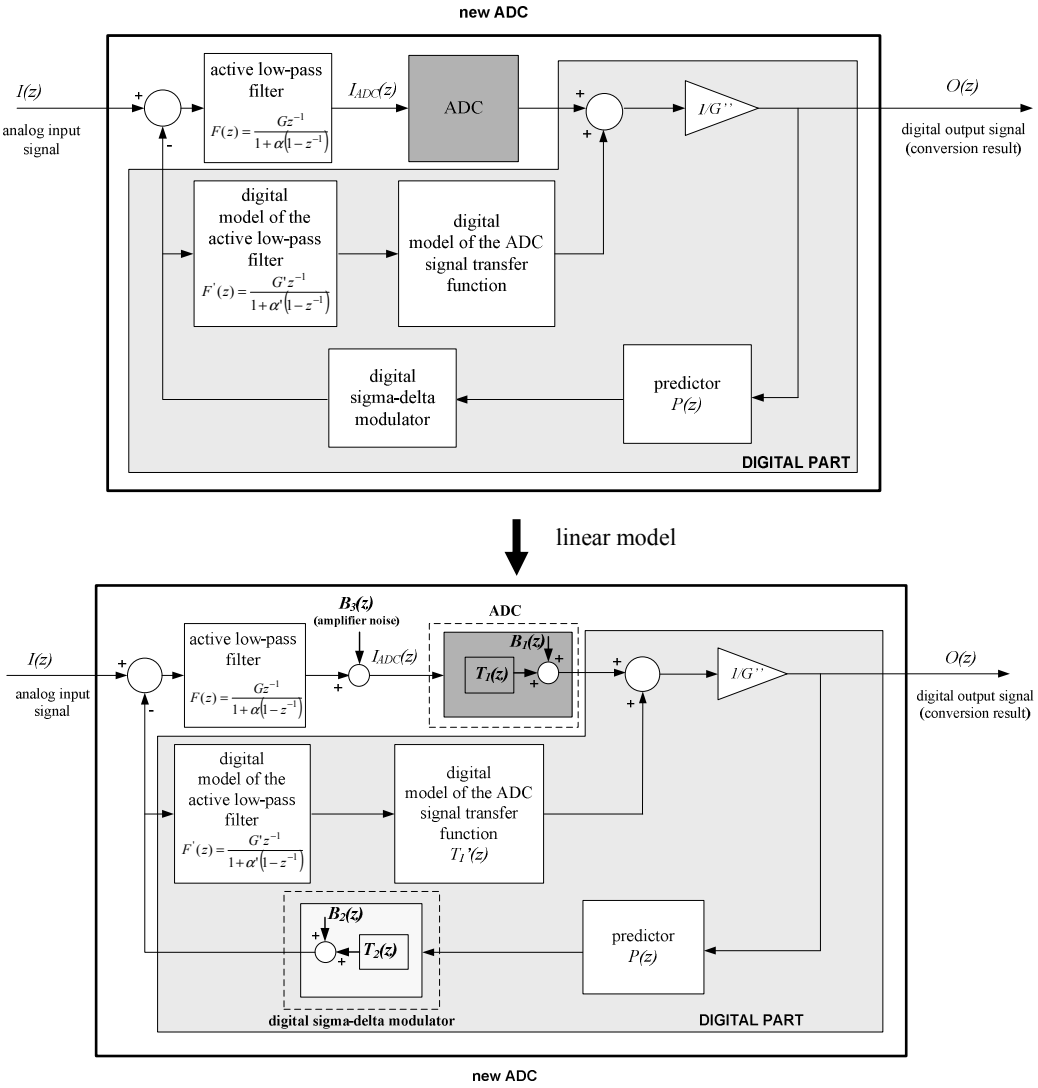


Fig. 4 Enhanced active topology

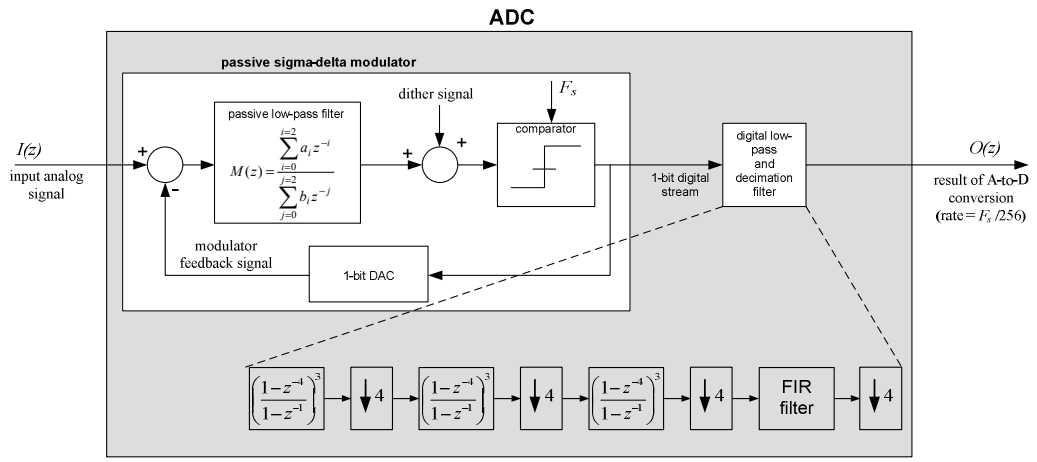


Fig. 5 A low-pass passive sigma-delta converter

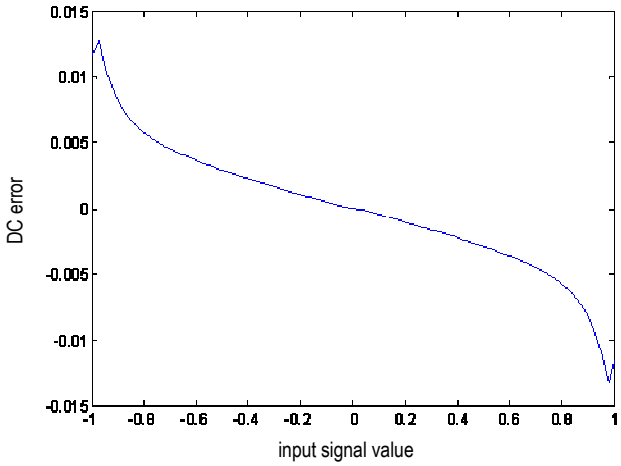


Fig. 6 - DC error of the passive sigma-delta ADC

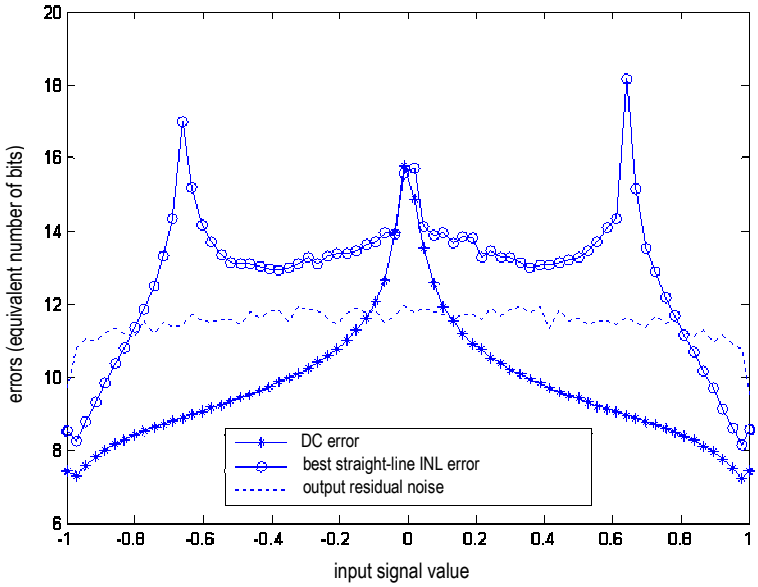


Fig. 7 DC error, INL error and output residual noise of the passive sigma-delta converter (in bits)

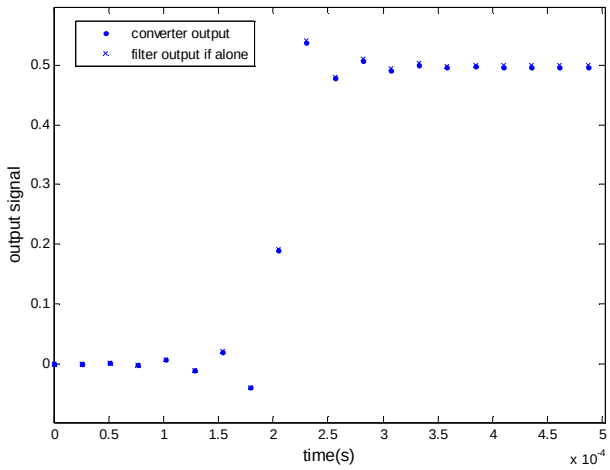


Fig. 8 Step response of the passive sigma-delta converter

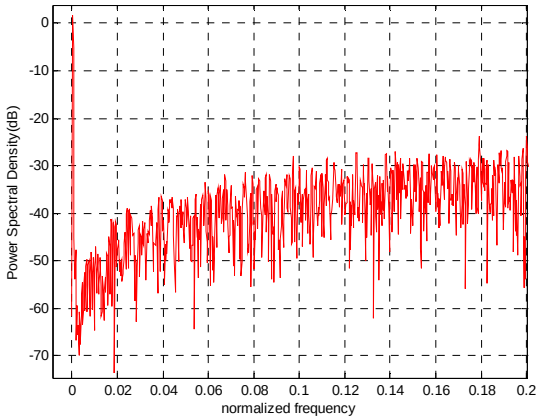
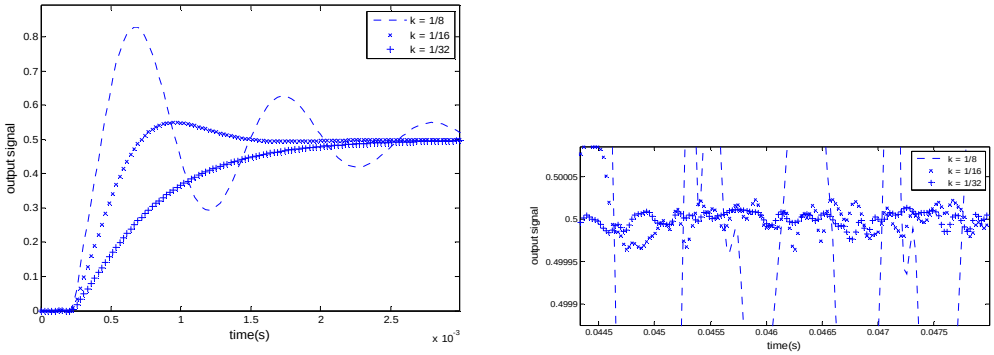


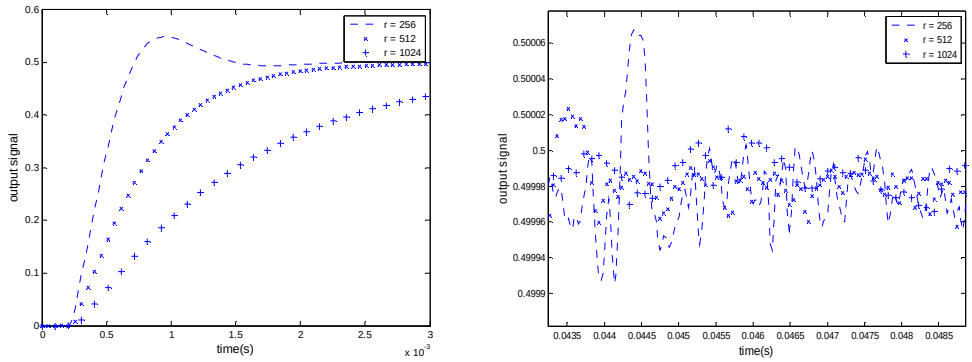
Fig. 9 Power Spectral Density of the passive modulator output



(a) (b)

Fig. 10 Passive loop topology: step response for different values of k (r = 256)

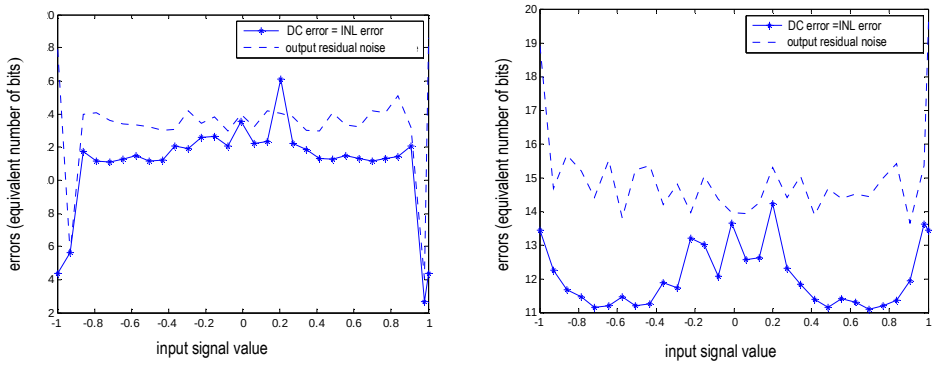
(a) transient period; (b) steady state



(a) (b)

Fig. 11 Passive loop topology: step response for different values of r (k = 1/16)

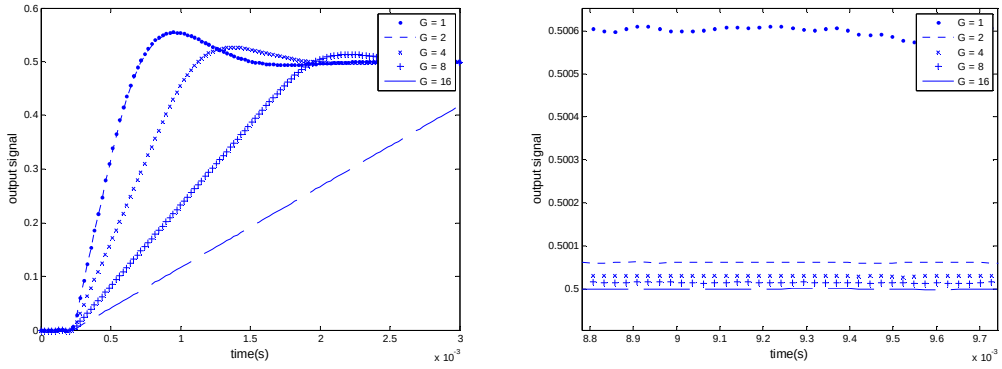
(a) transient period; (b) steady state



(a) (b)

Fig. 12 INL error and output residual noise of the passive loop topology (in bits)

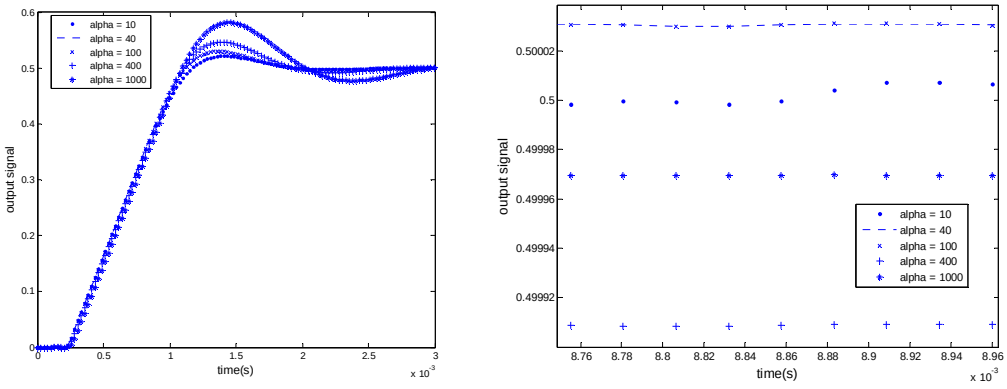
(a) $r = 256$; (b) $r = 512$



(a) (b)

Fig. 13 Active topology: step response for different values of G ($\alpha = 10$)

(a) transient period; (b) steady state



(a) (b)

Fig. 14 Active topology: step response for different values of α ($G = 4$)

(a) transient period; (b) steady state

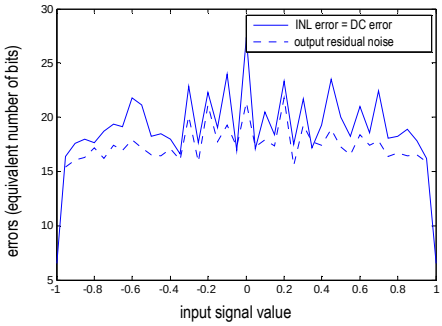


Fig. 15 INL error and output residual noise of the active topology (in bits)

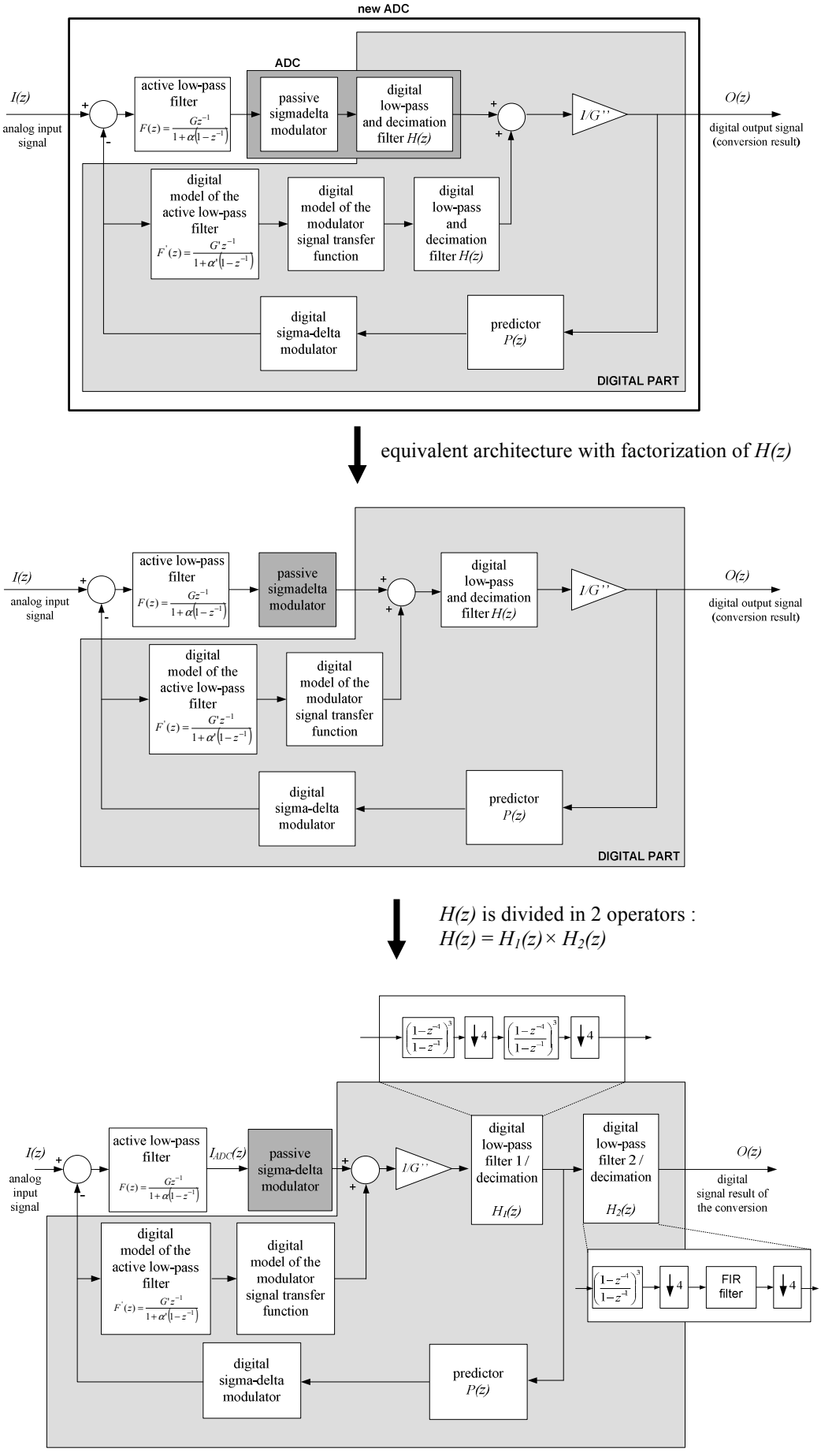


Fig. 16 Simulated enhanced active topology

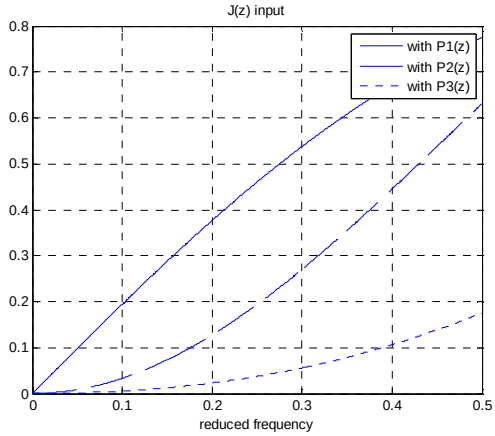


Fig. 17 $J(z)$ magnitude for (a) $P_1(z)$; (b) $P_2(z)$; (c) $P_3(z)$.

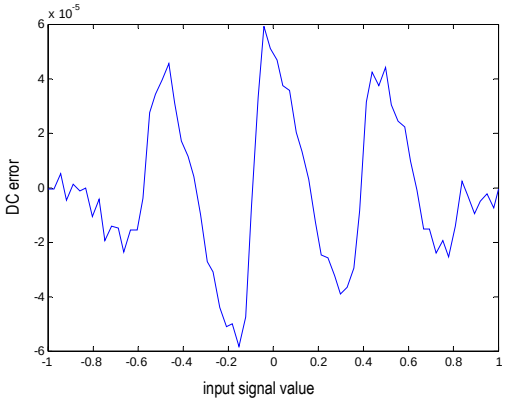


Fig. 18 DC error of the active enhanced topology

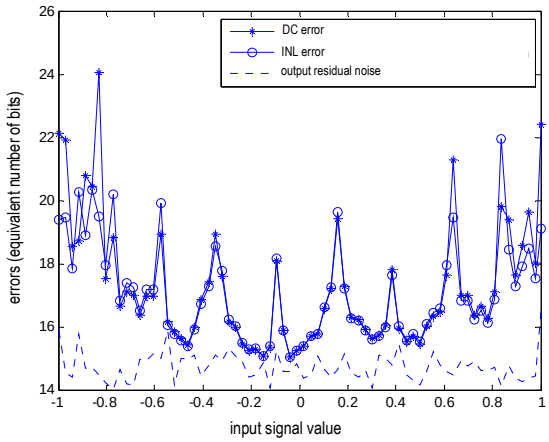


Fig. 19 DC error, INL error and output residual noise of the ideal enhanced active topology (in bits)

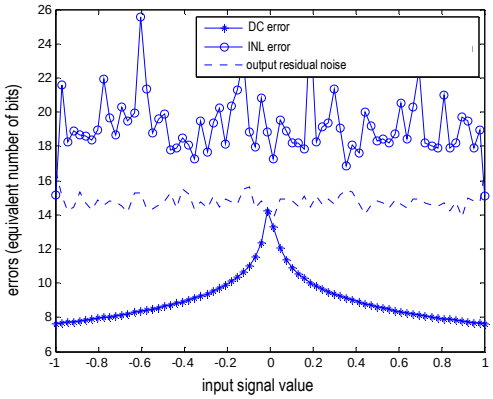


Fig. 20 DC error, INL error and output residual noise of the enhanced active topology (in bits): mismatch relative error of 1% in G''

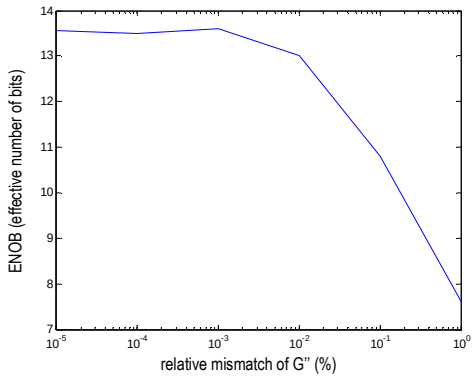


Fig. 21 Effect of a mismatch between G'' and $G'T'_{1\_DC}T_{2\_DC}$

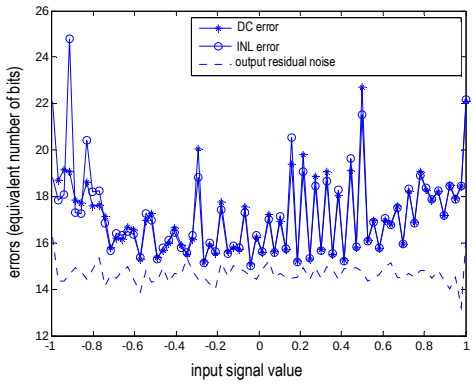
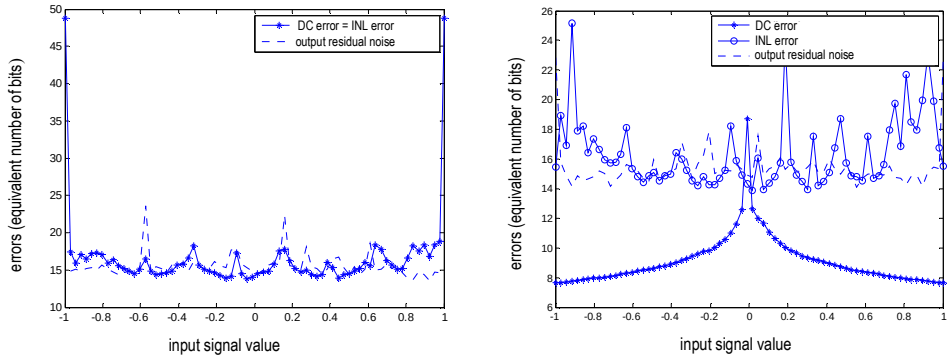


Fig. 22 DC error, INL error and output residual noise of the enhanced active topology (in bits): mismatch of 20% between the analog part and its digital model



(a) (b)

Fig. 23 DC error, INL error and output residual noise: influence of the CMRR of the active analog filter (a) CMRR=100dB; (b) CMRR=30dB

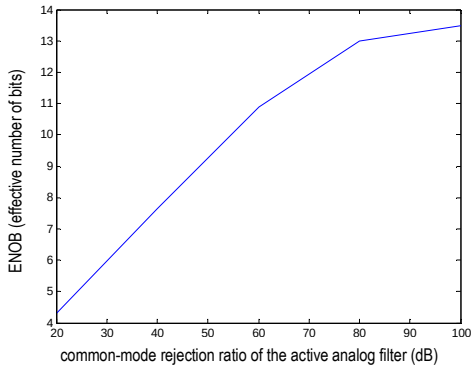
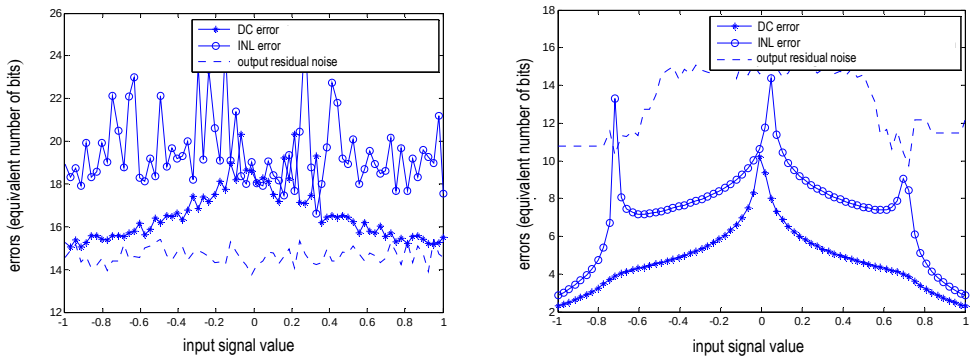
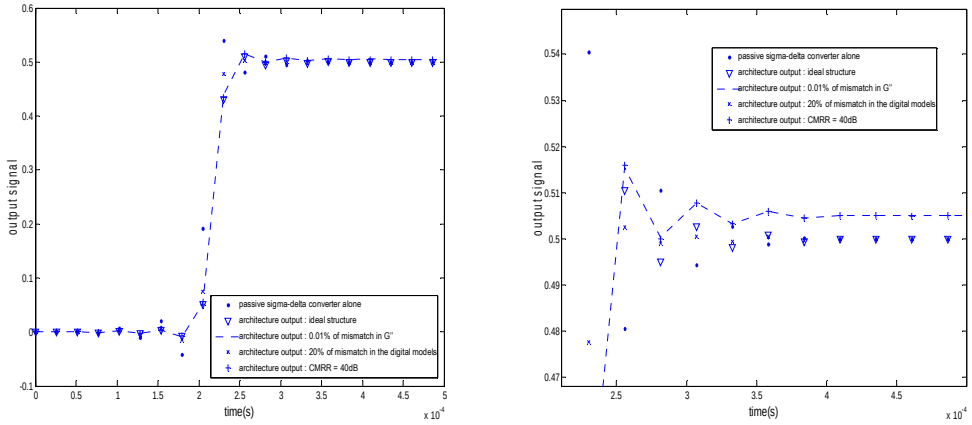


Fig. 24 ENOB (resolution) within the full range as a function of the CMRR of the active filter



(a) (b)

Fig. 25 DC error, INL error and output residual noise: CMRR = 40 dB
(a) ideal matching; (b) mismatch error of 20% in the digital models



(a) (b)

Fig. 26 Step response of the enhanced active topology

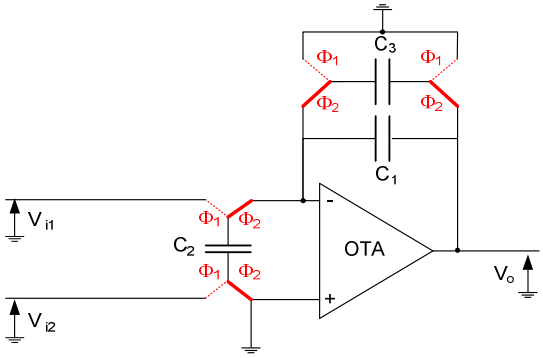


Fig. 27 Switched-capacitor active filter

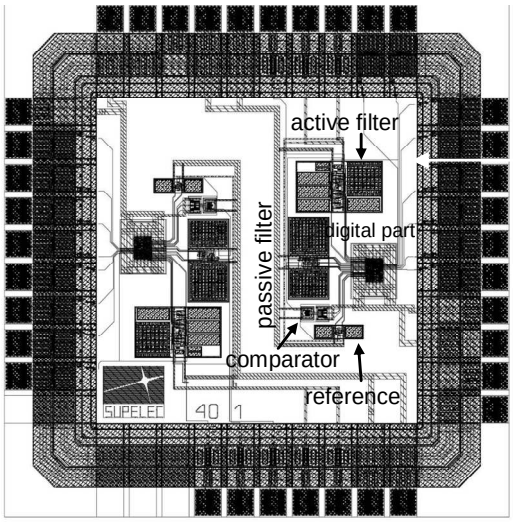
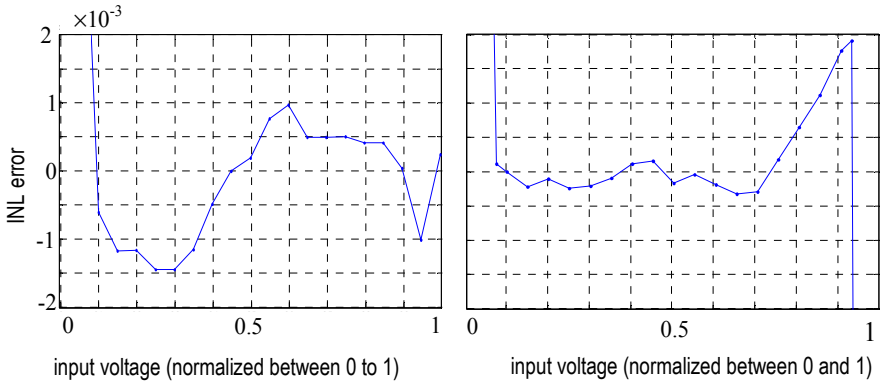


Fig. 28 Chip layout



(a) (b)

Fig. 29 INL measurement (enhanced active topology)

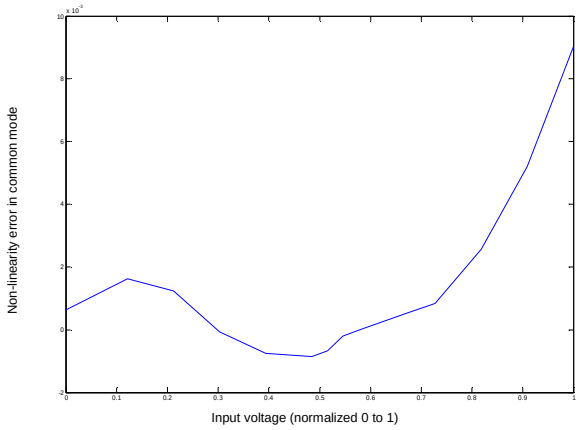


Fig. 30 Non-linearity of the common-mode gain

Table 1

	ENOB (Effective Number of bits)	Bandwidth
Passive sigma-delta ADC	8	16kHz
Passive sigma-delta ADC + linear post-correction	10	16kHz
Full passive topology	11	3 kHz
Active topology	15	3 kHz
Enhanced active topology	13	16kHz